In the Claims

Please cancel claims 9, 16 and 20.

Please amend claims 1, 5, 6, 8, 11-13 and 17-19 as follows.

1. (currently amended) An integrated circuit, comprising;

a semiconductor substrate;

an optical waveguide formed over the substrate;

an insulating planarization layer formed adjacent to the optical waveguide ~~and level with the top of the waveguide~~; ~~and~~

a microwave transmission line formed over the planarization layer and overlying a top surface of the optical waveguide, and

a semiconductor portion disposed adjacent to the optical waveguide to support the transmission line.

2. (original) A circuit as claimed in claim 1, wherein the insulating planarization layer comprises a tetra-ethyl-ortho-silicate (TEOS) layer.

3. (original) A circuit as claimed in claim 1, wherein the semiconductor substrate comprises a compound semiconductor.

4. (original) A circuit as claimed in claim 3, wherein the semiconductor is Gallium Arsenide-based.

5. (currently amended) A circuit as claimed in claim 1, wherein the optical waveguide ~~comprise~~ comprises a multiple layer structure, in which a substantially undoped Gallium Arsenide layer is sandwiched between substantially undoped Aluminium Gallium Arsenide layers.

6. (currently amended) A circuit as claimed in claim 1, comprising an electro-optic modulator, wherein two optical waveguide sections are formed over the substrate, and wherein a respective transmission line for each waveguide section is formed over the planarization layer.

7. (original) A circuit as claimed in claim 6, wherein the waveguide sections are parallel and spaced apart, the spacing between the waveguide sections being filled with the planarization layer.

8. (currently amended) A circuit as claimed in claim 6, wherein the waveguide sections are parallel and spaced apart, and wherein an air gap ~~being provided~~ is formed in the spacing between the waveguide sections.

9. (canceled).

10. (original) A circuit as claimed in claim 6, wherein a common conduction layer is provided beneath the waveguide sections.

11. (currently amended) A circuit as claimed in claim 6, wherein the insulating planarization layer comprises a tetra-ethyl-ortho-silicate (TEOS) layer.

12. (currently amended) A circuit as claimed in claim 6, wherein the semiconductor substrate is Gallium Arsenide-based.

13. (currently amended) A method of fabricating an integrated circuit, comprising;

providing a semiconductor substrate;

forming an optical waveguide over the semiconductor substrate;

~~depositing multiple semiconductor layers over the substrate;~~

~~patterning the multiple layers to define an optical waveguide stack formed over the substrate, the multiple layers being removed from the lateral sides of the waveguide stack;~~

depositing a planarization layer ~~to fill the sides of~~ adjacent to the optical waveguide ~~stack with a planarization layer to the same height as the waveguide stack~~; ~~and~~

forming a microwave transmission line over the planarization layer and contacting a top surface of the optical waveguide ~~stack~~, and

forming a semiconductor portion over the substrate and adjacent to the optical waveguide to support the transmission line.

14. (original) A method as claimed in claim 13, wherein the insulating planarization layer comprises a tetra-ethyl-ortho-silicate (TEOS) layer.

15. (original) A method as claimed in claim 13, wherein the semiconductor is Gallium Arsenide-based.

16. (canceled)

17. (currently amended) A method as claimed in claim 13 for fabricating an electro-optic modulator, further comprising forming ~~wherein the patterning of the multiple layers defines~~ two optical ~~waveguide stacks~~ waveguides, and wherein a respective transmission line for each waveguide ~~stack~~ is formed over the planarization layer.

18. (currently amended) A method as claimed in claim 17, wherein the ~~waveguide stacks~~ waveguides are parallel and spaced apart, and wherein the spacing between the waveguides ~~waveguide sections~~ is filled with the planarization layer.

19. (currently amended) A method as claimed in claim 17, wherein the planarization layer is not formed between the waveguides~~waveguide stacks~~.

20. (canceled)

Please add new claims 21-44 as follows.

21. (New) A circuit as claimed in claim 1, further comprising one or more air gaps formed in the circuit.

22. (New) A circuit as claimed in claim 1, wherein the planarization layer contacts at least a portion of the optical waveguide.

23. (New) A circuit as claimed in claim 1, wherein the planarization layer contacts at least a portion of the semiconductor portion.

24. (New) A circuit as claimed in claim 1, wherein the semiconductor portion comprises a bridge structure.

25. (New) A circuit as claimed in claim 1, further comprising a seed layer formed on at least a portion of the substrate and disposed between the substrate and the optical waveguide.

26. (New) A circuit as claimed in claim 25, further comprising a conduction layer formed on at least a portion of the seed layer and disposed between the seed layer and the optical waveguide.

27. (New) A circuit as claimed in claim 1, further comprising a conduction layer disposed between the substrate and the optical waveguide.

28. (New) A circuit as claimed in claim 1, wherein one end of the semiconductor portion contacts the optical waveguide and an opposed end contacts the planarization material.

29. (New) A circuit as claimed in claim 1, wherein the planarization layer is formed only on one side of the optical waveguide.

30. (New) A circuit as claimed in claim 6, wherein one end of the semiconductor portion contacts at least one of the optical waveguide sections, and an opposed end of the semiconductor portion contacts the planarization layer.

31. (New) A circuit as claimed in claim 6, wherein the planarization layer contacts at least a portion of the semiconductor portion.

32. (New) A circuit as claimed in claim 1, wherein the planarization layer is formed only on one side of the optical waveguide.

33. (New) A circuit as claimed in claim 6, wherein one end of the semiconductor portion contacts at least one of the optical waveguide sections, and an opposed end of the semiconductor portion contacts the planarization material.

34. (New) A method as claimed in claim 13, further comprising forming the optical waveguide by

depositing multiple semiconductor layers over the substrate, and

patterning the multiple layers to define an optical waveguide stack formed over the substrate, and

removing the multiple layers from lateral sides of the optical waveguide stack.

35. (New) A method as claimed in claim 34, wherein the multiple semiconductor layers forming the optical waveguide stack comprise a substantially undoped Gallium Arsenide layer sandwiched between substantially undoped Aluminium Gallium Arsenide layers.

36. (New) A method as claimed in claim 13, further comprising forming one or more air gaps in the circuit.

37. (New) A method as claimed in claim 17, further comprising forming an air gap between the two optical waveguides.

38. (New) A method as claimed in claim 13, wherein the planarization layer contacts at least a portion of the optical waveguide.

39. (New) A method as claimed in claim 13, wherein the planarization layer contacts at least a portion of the semiconductor portion.

40. (New) A method as claimed in claim 13, wherein the semiconductor portion comprises a bridge structure.

41. (New) A method as claimed in claim 13, further comprising forming a seed layer on at least a portion of the substrate, wherein the seed layer is disposed between the substrate and the optical waveguide.

42. (New) A method as claimed in claim 13, further comprising forming a conduction layer on at least a portion of the seed layer, the conduction layer is disposed between the seed layer and the optical waveguide.

43. (New) A method as claimed in claim 13, further comprising forming a conduction layer between the substrate and the optical waveguide.

44. (New) A method as claimed in claim 13, wherein one end of the semiconductor portion contacts the optical waveguide and an opposed end contacts the planarization layer.